Claims

1. A component, containing:

- a chip (CH) having electrically conductive structures on the underside of the chip,

- a carrier substrate (TS), which has connecting areas (AF) on the surface, with the chip (CH) being mounted in flip chip arrangement on the carrier substrate by means of electrically conductive connections (BU), and with the connecting areas (AF) being electrically connected to the electrically connective structures of the chip by means of electrically conductive connections (BU),

- a support element (SE) to relieve the electrically conductive connections, which is positioned on the top side of the carrier substrate and encircles the chip without touching it,

- a seal (AB) which surrounds the chip and tightly closes at least the space between the support element and the aforementioned chip, with the seal being supported on this support element.

2. The component as recited in claim 1, wherein the electrically conductive connections are bumps.

3. The component as recited in claim 1 or 2, wherein the seal (AB) is designed as a dielectric layer which also covers the top side of the chip.

4. The component as recited in claim 3, wherein the dielectric layer consists of one or more layers.

5. A component, containing:

- a chip (CH) having electrically conductive structures on the underside of the chip,

- a carrier substrate (TS), which has connecting areas (AF) on the surface, with the chip (CH) being mounted in flip chip arrangement on the carrier substrate by means of electrically conductive connections (BU), and with the connecting areas (AF) being electrically connected to the electrically connective structures of the chip by means of electrically conductive connections (BU),

with a composite of a dielectric layer and a metal layer over it being positioned on the top side of the chip, with this composite being sealed to the carrier substrate outside of the chip area, and with the chip thickness being selected so that the forces arising due to thermal expansion of the aforementioned composite in the temperature range between -60° C and 85° C per one electrically conductive connection or bump are a maximum of 2 Newtons.

6. A component, containing:

- a chip (CH) having electrically conductive structures on the underside of the chip,

- a carrier substrate (TS), which has connecting areas (AF) on the surface, with the chip (CH) being mounted in flip chip arrangement on the carrier substrate by means of electrically conductive connections (BU), and with the connecting areas (AF) being electrically connected to the electrically connective structures of the chip by means of electrically conductive connections (BU),

- with a composite of a dielectric layer and above it a metal layer positioned on the top side of the chip, with this composite forming a seal with the carrier substrate around the chip outside of the chip surface, and

- with the dielectric layer having a modulus of elasticity of less than 1 Gpa, a thickness of less than 20 μm or a coefficient of thermal expansion which is greater than $\alpha_{bump}/2$ and less than 2 α_{bump}, where α_{bump} is the coefficient of thermal expansion of the electrically conductive connections (BU).

7. A component, containing:

- a chip (CH) having electrically conductive structures on the underside of the chip,

- a carrier substrate (TS), which has connecting areas (AF) on the surface, with the chip (CH) being mounted in flip chip arrangement on the carrier substrate by means of electrically conductive connections (BU), and with the connecting areas (AF) being electrically connected to the electrically connective structures of the chip by means of electrically conductive connections (BU),

- a support element located on the top side of the carrier substrate in the form of a

shrink frame, which encircles the chip and tightly encloses it.

8. The component as recited in claim 7, wherein there is a metal layer that covers the top side of the chip and the shrink frame and forms a seal with the carrier substrate.

9. The component as recited in one of claims 1 through 8, wherein the side surfaces of the chip (CH) are sloped, so that the cross section of the chip tapers toward the carrier substrate (TS).

10. The component as recited in one of claims 1 through 9, wherein the side surfaces of the chip (CH) have at least one step.

11. The component as recited in one of claims 1, 2, 9 or 10, wherein the seal covers the edge areas of the chip and of the support element surrounding it, with the top side of the chip not being covered by the seal.

12. The component as recited in one of claims 1, 2 or 9 through 11, wherein there is a metal layer (ME) on the top side of the chip, on the seal (AB), and on edge areas of the support element and/or of the carrier substrate that adjoin the seal and are not covered by it.

13. The component as recited in one of claims 3, 4, 9 or 10, wherein the dielectric

layer (AB) completely covers the chip (CH) together with the support element (SE) that encircles it, with this dielectric layer lying on the top side of the chip and on the support element and forming a seal with the carrier substrate only outside of the support element, so that the chip and the support element encircling it are in a shared cavity which is formed between the dielectric layer and the top side of the carrier substrate.

14. The component as recited in one of claims 3, 4, 9 or 10, wherein the dielectric layer (AB) completely covers the top side of the chip and seals it to the support element, with the support element being of a hermetically tight material.

15. The component as recited in one of claims 3 through 6, 9, 10, 13 or 14, wherein there is a metal layer (ME) that covers at least the dielectric layer and forms a composite with it.

16. The component as recited in one of claims 3 through 6, 9, 10 or 13 through 15, wherein there is a filling compound on the dielectric layer or on the composite of the dielectric layer and the metal layer outside of the chip.

17. The component as recited in claim 16, wherein the metal layer forms a seal with the support element outside of the chip area, or with the carrier substrate outside of the support element.

18. The component as recited in claim 9 or 10, wherein there is contact metallization (KM) on the side surfaces of the chip which face toward the carrier substrate (TS) or are sloping,

wherein the support element (SE) is in the form of a solder frame on the top side of the carrier substrate, with the support element being soldered to the contact metallization of the chip, and with the seal (AB) being formed by the solder frame.

19. The component as recited in claim 18, wherein the top side of the chip is provided with a metal layer.

20. The component as recited in at least one of claims 1, 2, 11 or 12, wherein the seal is made of a dielectric material.

21. The component as recited in claim 20, wherein the seal is made of a plastic, an organic plastic, a laminate film, a glass solder or a resin.

22. The component as recited in one of claims 3, 4, 9, 10, 13 through 17, wherein the dielectric layer is made of a plastic, an organic plastic, a laminate film, a glass solder or a resin.

23. The component as recited in at least one of claims 1 through 4, 9 through 17 or 20 through 22, wherein the support element is made of metal, a ceramic material or

plastic.

24. The component as recited in one of claims 1 through 4, 9 through 17 or 20 through 22, wherein the support element is the boundary of an indentation provided on the carrier substrate.

25. The component as recited in one of claims 1 through 4 or 9 through 24, wherein the height of the support element does not exceed the distance between the top side of the carrier substrate and the bottom edge of the chip, with the inner edge of the support element reaching under the edge of the chip that is directed toward the carrier substrate.

26. The component as recited in at least one of claims 1 through 4, 9 through 17 or 20 through 24, wherein the height of the support element is equal to the distance between the top side of the carrier substrate and the bottom edge of the chip or exceeds this distance.

27. The component as recited in one of claims 1 through 26, wherein the carrier substrate (TS) is an LTCC ceramic - low temperature cofired ceramic.

28. The component as recited in one of claims 1 through 27, wherein there are SMD-capable external contacts (AK) on the underside of the carrier substrate (TS).

29. The component as recited in one of claims 1 through 28, wherein the carrier substrate (TS) includes at least two dielectric layers.

30. The component as recited in one of claims 1 through 29, wherein the chip (CH) contains at least one resonator that works with acoustic surface waves or acoustic volume waves.

31. The component as recited in one of claims 1 through 30, which includes a plurality of like or differing chips, with the chips being attached on the carrier substrate (TS) and encapsulated in the same manner.

32. A method for producing an encapsulated component,

- wherein a chip with sloping side surfaces that tapers toward the surface which bears electrically conductive structures or a chip with side surfaces that have at least one step is used, with the side surfaces of the chip having contact metallization,

- wherein there is metallization on the top side of a carrier substrate for placing a solder frame,

- wherein the solder frame is produced on the carrier substrate,

- wherein the chip is placed on the carrier substrate and is soldered to it in flip chip construction,

- wherein the solder frame is soldered to the contact metallization on the side surfaces

of the chip.

33. The method as recited in claim 32, wherein prior to soldering the chips to the solder frame, insulating non-wettable structures IS are applied onto the chip between the contact metallization of the side surfaces and the electrically conductive structures.

34. The method as recited in claim 32 or 33, wherein a metal layer is applied to the top side of the chip.

35. A method for producing an encapsulated component,

- wherein a chip is used which has a surface with electrically conductive structures,

- wherein a substrate is used which has on its top side connecting areas for making contact with the chip and a frame with a shrinkage behavior,

- wherein the chip is placed on the carrier substrate and is soldered to it in flip chip construction,

- wherein the frame is produced before the chip is placed on the carrier substrate,

- wherein the frame is shrunk through temperature handling so that it tightly encloses the chip,

- wherein a metal layer is produced which completely covers the top side of the chip and the shrink frame.

36. The method as recited in claim 35,

- wherein one side of the frame is provided with a solderable layer or with an adhesive

layer,

- wherein the frame is connected with the carrier substrate by means of the aforementioned layer.

37. A method for producing an encapsulation for an electric component with the following processing steps:

- at least two chips carrying conductive structures are attached by means of electrically conductive connections (SU) in flip chip arrangement to a carrier substrate (TS), which has on its surface connecting areas (AF) for electrical connection with the electrically conductive structures of the chip,

- the at least two chips (CH) are covered with a dielectric layer (AB) which lies on the top side of the chip and seals it together with the carrier substrate, so that in this way each of the at least two chips is individually encapsulated,

- the space between the at least two chips is filled with a filling compound (VM).

38. The method as recited in claim 37,

- wherein a metal layer (ME) that forms a composite with the dielectric layer (AB) is applied to the dielectric layer,

- wherein the filling compound (VM) is applied to the composite of the dielectric layer and the metal layer outside of the chip.

39. The method as recited in claim 37 or 38, wherein the carrier substrate is then

be sawed apart, so that individual components result which include at least one of the aforementioned chips.